

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

<div>TQ DELTA, LLC,</div> <div style="text-align: right;">Plaintiff,</div> <div style="text-align: center;">v.</div> <div>2WIRE, INC.</div> <div style="text-align: right;">Defendant.</div>	Civil Action No. 13-cv-1835-RGA
<div>TQ DELTA, LLC,</div> <div style="text-align: right;">Plaintiff,</div> <div style="text-align: center;">v.</div> <div>ZYXEL COMMUNICATIONS, INC. and ZYXEL COMMUNICATIONS CORPORATION,</div> <div style="text-align: right;">Defendants.</div>	Civil Action No. 13-cv-2013-RGA
<div>TQ DELTA, LLC,</div> <div style="text-align: right;">Plaintiff,</div> <div style="text-align: center;">v.</div> <div>ADTRAN, INC.</div> <div style="text-align: right;">Defendant.</div>	Civil Action No. 14-cv-954-RGA
<div>ADTRAN, INC,</div> <div style="text-align: right;">Plaintiff,</div> <div style="text-align: center;">v.</div> <div>TQ DELTA, LLC.</div> <div style="text-align: right;">Defendant.</div>	Civil Action No. 15-cv-121-RGA

**[PROPOSED] CLAIM CONSTRUCTION ORDER FOR
FAMILY 3 PATENTS**

The Court has determined that the terms below shall be given the following meaning for U.S. Patent Nos. 7,831,890 (“the ’890 patent”), 7,836,381 (“the ’381 patent”), 7,844,882 (“the ’882 patent”), 8,276,048 (“the ’048 patent”), 8,495,473 (“the ’473 patent”), and 8,607,126 (“the ’126 patent”):¹

1. **“shared memory”** – “common memory used by at least two functions, where a portion of the memory can be used by either one of the functions”
2. **“amount of memory”** – plain meaning
3. **“the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]”** – “the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory”
4. **“latency path”** – “transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay”
5. **“wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the message”** – plain meaning
6. **“portion of memory”** – plain meaning
7. **“memory is allocated between the [first] interleaving function and the [second interleaving / deinterleaving] function”** – “an amount of the memory is allocated to the [first] interleaving function and an amount of memory is allocated to the [second interleaving / deinterleaving] function”

¹ The Court has not announced a meaning for the term “transceiver.”

8. **“wherein the generated message indicates how the memory has been allocated between the [first deinterleaving / interleaving] function and the [second] deinterleaving function”** – “wherein the generated message indicates the amount of memory that has been allocated to the [first deinterleaving / interleaving] function and the amount of memory allocated to the [second] deinterleaving function”

IT IS SO ORDERED this _____ day of December, 2017.

The Honorable Richard G. Andrews